2823 AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

#22/Appeal Brief
10/26/01
V. Vannucci

In re the Application of

Yasunori INOUE et al.

Serial Number: **09/228,148** Group Art Unit: **2823**

Filed: **January 11, 1999** Examiner: **K. Eaton**

For: **SEMICONDUCTOR DEVICE INCLUDING AN INSULATING FILM ON A CONDUCTIVE LAYER AND MANUFACTURING METHOD THEREOF**

SUBMISSION OF APPEAL BRIEF

Commissioner for Patents
Washington, D.C. 20231

October 22, 2001

Sir:

Submitted herewith are an original and two copies of an Appeal Brief in the above-identified U.S. patent application.

Also enclosed is a check in the amount of $320.00 to cover the cost of filing this Appeal Brief. In the event that any additional fees are due with respect to this paper, please charge Deposit Account No. 01-2340. This paper is filed in triplicate.

Respectfully submitted,

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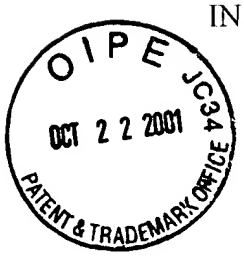
Enclosures: Duplicate of this paper; Appeal Brief and two copies; and check for $320.00



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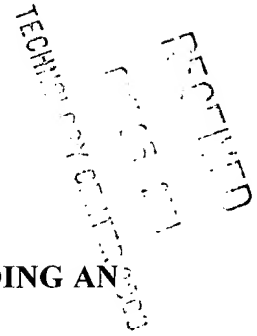

APPEAL BRIEF FOR THE APPELLANT

Ex parte **Yasunori INOUE et al.** (applicants)

MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE INCLUDING AN INSULATION FILM ON A CONDUCTIVE (AS AMENDED)

Serial Number: **09/228,148**

Filed: **January 11, 1999**

Appeal No. :

Group Art Unit: **2823**

Examiner: **K. Eaton**

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BRIEF ON APPEAL

(I) REAL PARTY IN INTEREST

The real party in interest is **Sanyo Electric Co., Ltd**, by an assignment recorded in the U. S. Patent and Trademark Office on **February 26, 1997**, at Reel **8407**, Frame **0832**.

(II) RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to appellant, appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(III) STATUS OF CLAIMS

Claims 9-18 are pending. Claims 9-18 are appealed. The appealed claims are reproduced in the attached Appendix.

(VI) STATUS OF AMENDMENTS

No amendments have been filed subsequent to final rejection.

(V) SUMMARY OF THE INVENTION

The invention is directed to an method of manufacturing a semiconductor device with improved planarization as well as reliability. The present invention is characterized by providing

a film for substantially preventing intrusion of impurities into a conductive layer. The film preventing intrusion is formed between a first insulation film and a conductive layer. By forming the first insulation film including impurities on the conductive layer, the first insulation film is modified to have moisture and hydroxyl group reduced. Furthermore, the provision of a film between the first insulation film and the conductive layer effectively prevents the impurities of the first insulation film from entering the conductive layer. Thus, the disadvantage of a shorter electromigration lifetime of the conductive layer before disconnection due to intrusion of the impurities of the first insulation layer into the conductive layer can be prevented. See page 5, line 5 through page 9, line 10 of the specification.

Claim 9 sets forth the steps of:

forming a first insulation film on a conductive layer formed on a substrate,

introducing impurities into said first insulation film, and

forming an intrusion prevention film to substantially prevent the impurities introduced into said first insulation film form entering said conductive layer prior to said step of forming said first insulation film.

The steps set forth in independent claim 18 are similar to claim 9, with the exception that claim 18 specifies the materials which may be employed for the film for substantially preventing impurities from intruding into the conductive layer, and requires patterning of the conductive layer and the intrusion prevention film.

(VI) ISSUES

The following issues are presented on appeal:

1) Whether claims 9-13 and 15-18 are unpatentable under 35 USC § 103(a) over the combination of ***Leong*** in view of ***Wolf et al.***; and

2) Whether claim 14 is unpatentable under 35 USC § 103(a) as being unpatentable over the combination of ***Leong*** in view of ***Wolf et al.*** and further in view of ***Wolf***.

(VII) GROUPING OF THE CLAIMS

For each ground of rejection, the claims may be considered to stand or fall together. However, it is believed that claim 18 is separately patentable for the reasons given in the Argument.

(VIII) ARGUMENT

(1)(a) Claims 9-13 and 15-18 are patentable over ***Leong*** in view of ***Wolf et al.***

As set forth in the Office Action dated October 11, 2000, ***Leong*** shows a first insulation film 24 on a conductive layer 20 formed on a substrate 10. Impurities are introduced into the insulation film 24. Furthermore, ***Leong*** does not show forming a film to substantially prevent impurities introduced into the first insulation film from entering the conductive layer.

As also set forth in the Office Action dated October 11, 2000, ***Wolf et al.*** discloses a titanium tungsten material used in a lithography process. More specifically, ***Wolf et al.*** discusses

the use of a type of anti-reflective layer coating (ARC) which is highly absorbing and non-bleaching at an exposure wavelength in resist processing. ***Wolf et al.*** discusses the need to reduce the effects of standing wave interference and light scattering, especially over highly reflective substrates, in photoresists. Although such ARCs can substantially reduce standing wave effects, such increases process complexity and possibly loss of dimensional control.

The Examiner argues that one of ordinary skill in the art would have found it obvious to have modified the disclosure of ***Leong*** based on the teachings of ***Wolf et al.*** Appellant respectively disagrees.

The insulation film 24 of ***Leong*** is a SOG for planarization of an integrated circuit device. In contrast, ***Wolf et al.*** is directed to a photoresist material. Based on this difference, one of ordinary skill in the art would not have been motivated to look to the teachings of ***Wolf et al.*** and have modified ***Leong*** as asserted by the Examiner. More specifically, a photoresist has different properties and functions than a SOG. In particular, a photoresist is required to have particular properties for patterning whereas SOG is used for planarization. Thus, when patterning, standing wave effects as taught by ***Wolf et al.*** would be a consideration during patterning.

In contrast thereto, the SOG taught by ***Leong*** is for planarization. Ion implantation is employed to cure the SOG layer by heating (see column 4, lines 1-20 of Leong). It is only after the SOG layer has been cured in which openings can be made "using conventional lithography and etching techniques" (column 4, lines 1-24). As such, there is no reason for one of ordinary skill in the art to have been motivated to modify Leong by the disclosure of Wolf et al. as asserted by the Examiner. As such, the combination of ***Leong*** and ***Wolf et al.*** fails to raise a prima facie rejection of the claims.

(1)(b) Claim 18 is separately patentable

Claim 18 is separately patentable. In particular, claim 18 requires the step of patterning said conductive layer and said intrusion prevention film. There is no teaching or suggestion provided by ***Leong*** and ***Wolf et al.*** of this step.

Furthermore, claim 18 requires the step of forming a first insulation film on said patterned conductive layer and intrusion prevention film. ***Leong*** and ***Wolf et al.*** also fail to provide any teaching or suggestion of this particular step. That is, the combination of ***Leong*** and ***Wolf et al.*** does not teach forming a first insulation film on a patterned conductive layer and intrusion prevention film.

Lastly, the combination of ***Leong*** and ***Wolf et al.*** fails to teach or suggest the step of implanting impurities into the first insulation film (which has been formed on the patterned conductive layer and intrusion prevention film).

(2)(a) Claim 14 is patentable over ***Leong***, ***Wolf et al.*** and ***Wolf***

In the Office Action dated October 11, 2000, the Examiner acknowledged that the combination of ***Leong*** and ***Wolf et al.*** does not show that the first insulation film includes silicon oxide containing at least 1% of carbon. ***Wolf*** was applied by the Examiner for its disclosure the SOG films can contain at least 1% of carbon.

Wolf fails to remedy the deficiencies of ***Leong*** and ***Wolf et al.*** as discussed above. That is, there is no motivation to combine ***Leong*** and ***Wolf et al.*** as asserted by the Examiner. Thus, the Examiner has failed to raise a prima facie rejection of claim 14.

(IX) CONCLUSION

For all of the above reasons, this Honorable Board is respectfully requested to reverse the rejections of the Primary Examiner.

In the event this paper is not timely filed, appellant hereby petitions for an appropriate extension of time. The fee for any such extension may be charged to our Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

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Attachment: Appendix

APPENDIX

9. A method of manufacturing a semiconductor device comprising the steps of:

forming a first insulation film on a conductive layer formed on a substrate,

introducing impurities into said first insulation film, and

forming an intrusion prevention film to substantially prevent the impurities introduced into said first insulation film from entering said conductive layer prior to said step of forming said first insulation film.

10. The manufacturing method of a semiconductor device according to claim 9, wherein said intrusion prevention film includes at least one material selected from the group consisting of silicon oxide, silicon nitride, Ti, TiN, W, WN_x and TiW.

11. The method of manufacturing a semiconductor device according to claim 9, further comprising the step of forming a second insulation film on said conductive layer and said intrusion prevention film prior to said step of forming the first insulation film.

12. The method of manufacturing a semiconductor device according to claim 11, wherein said second insulation film includes a film less hygroscopic than said first insulation film.

13. The method of manufacturing a semiconductor device according to claim 9, further comprising the step of forming a third insulation film on said first insulation film after said step of implanting impurities into the first insulation film.

14. The method of manufacturing a semiconductor device according to claim 9, wherein said first insulation film includes silicon oxide containing at least 1% of carbon.

15. The method of manufacturing a semiconductor device according to claim 9, wherein said first insulation film includes an inorganic SOG film.

16. The method of manufacturing a semiconductor device according to claim 9, wherein said step of introducing impurities is carried out by ion implantation.

17. The method of manufacturing a semiconductor device according to claim 9, wherein said impurities include at least one element selected from the group consisting of argon, boron, nitrogen, and phosphorus.

18. A method of manufacturing a semiconductor device comprising the steps of:

forming a conductive layer on a substrate,

forming a film on said conductive layer, said film including at least one material selected from the group consisting of silicon oxide, silicon nitride, Ti, TiN, W, WN_x and TiW, for substantially preventing impurities implanted from above of said conductive layer from intruding into said conductive layer,

patterning said conductive layer and said intrusion prevention film,

forming a first insulation film on said patterned conductive layer and intrusion prevention film, and

implanting impurities into said first insulation film.